13.5 11Gb/s Monolithically Integrated Silicon Optical Receiver for 850nm Wavelength

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The increasing bandwidth demand of future applications requires low-cost multi-Gb/s data links. With the development of VCSELs at a short wavelength of 850nm, silicon can be used to realize effective detectors. This leads to the possibility of realizing fully monolithically integrated silicon optical receivers including a photodiode with amplifier and optionally additional signal- and data-processing blocks with the advantage of eliminating interconnect capacitances between photodiode and amplifier. Additionally, the integrated approach opens the way to optical receivers for massively parallel optical interconnects.

A previous publication [1] of a monolithically integrated optical receiver implemented an avalanche photodiode together with an amplifier in a 0.13µm SOI process. At a maximum data rate of 8Gb/s, it reached a sensitivity of only +2dBm for a BER of 10^{-9}. In [2], a silicon optical receiver was realized with an external lateral silicon pin photodiode. For a BER of 10^{-9}, it reached sensitivities of -8.6dBm and -6.9dBm at 8Gb/s and 10Gb/s, respectively. These two realizations use avalanche gain of the photodiode to reach the highest possible sensitivity in this technology, making it not a robust choice for mass-market applications. In the proposed design, a modified 0.5µm BiCMOS process with f_T=25GHz that offers a vertical pin photodiode is used. This technology was also used for an optical receiver IC for DVD-applications published in [3], proving its reliability, robustness, and cost-effectiveness for mass-market applications. Without the need for an avalanche gain, the proposed optical receiver reaches sensitivities of -10.8, -10.2, -9, and -6.9dBm for data rates of 8, 10, 11, and 11.5Gb/s respectively, at a wavelength of 850nm,with a BER of $10^{-9,}$ and a PRBS with a length of 2^{15}-1. With a PRBS with the length of 2^{31}-1 and under the same conditions, sensitivities of -10.8, -10.1, and -8.9dBm for data rates of 8, 10, and 11Gb/s could be measured with a bit error analyzer. Compared to [1] the sensitivity is enhanced by 12.8dB at 8Gb/s, and compared to the nonmonolithical solution [2] by 2.2dB at 8Gb/s and by 3.2dB at 10Gb/s.

A vertical pin photodiode (Fig. 13.5.1) with a diameter of 50µm and a thickness of 10µm is used as a detector offering a responsivity of 0.26A/W at 850nm and a very low capacitance of 60fF. This type of photodiode first proposed by [4] offers the advantage that a higher voltage than the circuit voltage can be applied to the photodiode. Another advantage is that charge carriers that are generated in the substrate due to the deep penetration of the infrared light are effectively shielded due to the field between the cathode and the substrate, leading to only small diffusion tails in the order of 12% generated from carriers in the cathode itself. The 3dB cut-off frequency of the photodiode at a reverse voltage of V_{PH}=17V and a wavelength of 850nm is determined to be 2.2GHz.

To enable high-speed data reception above about 4Gb/s, the frequency response of the diode must be corrected with the help of an analog equalizer. Equalization of the photocurrent was successfully demonstrated with an n-well/p-substrate diode in [5] enhancing the data rate of a standard CMOS optical receiver up to 3Gb/s. Due to the high cut-off frequency of the pin photodiode, the speed could be further enhanced to more than 11Gb/s with the equalizer. Compared to [5] only two main poles and one zero have to be compensated, the first pole-zero combination exists due to charge carrier generation in the cathode generating slow diffusion tails and the second pole exists due to the drift time in the intrinsic zone.

The simplified schematic, but with the detailed front-end of the complete optical receiver, can be seen in Fig. 13.5.2. The photocurrent is converted to a voltage with a transimpedance amplifier (TIA) (T1, T3, R1, R3, R5, C1, C3, and Rfb1) that has a transimpedance of 500Ω. This voltage minus a reference voltage is amplified with a frequency-dependent characteristic that is proportional to the inverse characteristic of the photodiode response. This is done with a cascoded difference amplifier (T5, T6, T7, T8, R7, and R8) that has frequency-dependent coupling elements. The drift time of the photodiode is compensated with Rd and Cd and the small diffusion part is compensated with Cl, Rl1, and Rl2. After the equalizing amplifier, the overall transfer function has a nearly flat frequency response and linear phase. A three-stage limiting amplifier follows to improve the gain, limit the signal amplitude, and to drive a differential 100Ω load. There exists also a controlling circuit that generates together with a differential integrator and a dummy TIA (T2, T4, R2, R4, R6, C2, and Rfb2) the reference voltage for the equalizing amplifier by injecting the average photocurrent I_{AVG} into the dummy TIA via Rc. This ensures symmetrical clipping of the "0"s and "1"s in case of optical overdrive. The controlling circuit introduces a lower cut-off frequency of 30kHz eliminating the influence of background light.

Figure 13.5.3 shows the measured small-signal frequency response at a wavelength of 850nm with an upper-3dB cut-off frequency of 7.7GHz. Together with an overall transimpedance of 3kΩ, this leads to a transimpedance bandwidth product of 23THzΩ. The BER is measured with a bit error analyzer for different data rates, optical power levels, and two different lengths of the PRBS. The results can be seen in Fig. 13.5.4. An eye diagram at 11Gb/s and a PRBS of 2^{31}-1 at minimum optical power of -8.9dBm for a BER of 10^{-9} is shown in Fig. 13.5.5.

In Fig. 13.5.6, the chip micrograph is shown. It includes the 50µm pin photodiode that matches to a 50µm multimode fiber. The whole chip including bond pads and supply blocking capacitors occupies an area of 870µm × 700µm. The power consumption of the whole chip including the 100Ω driver at a supply voltage of 5V is 310mW.

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References:
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[5] S. Radovanovic, A.-J. Annema, B. Nauta, "3Gb/s Monolithically Integrated Photodiode and Pre-Amplifier in Standard 0.18µm CMOS," *ISSCC Dig. Tech. Papers*, pp. 472-473, Feb., 2004.

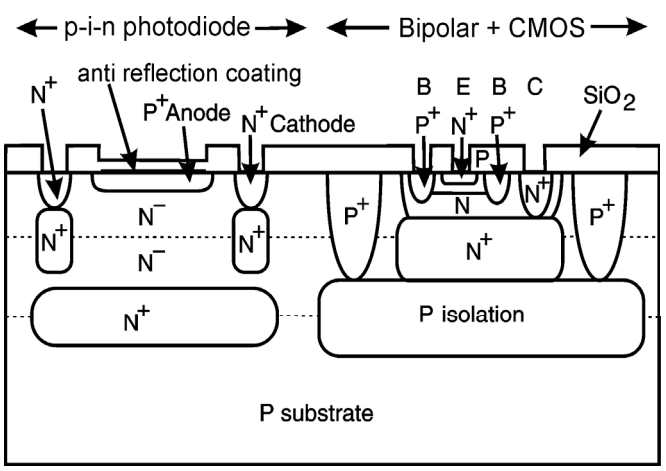

Figure 13.5.1: Cross section of the receiver.

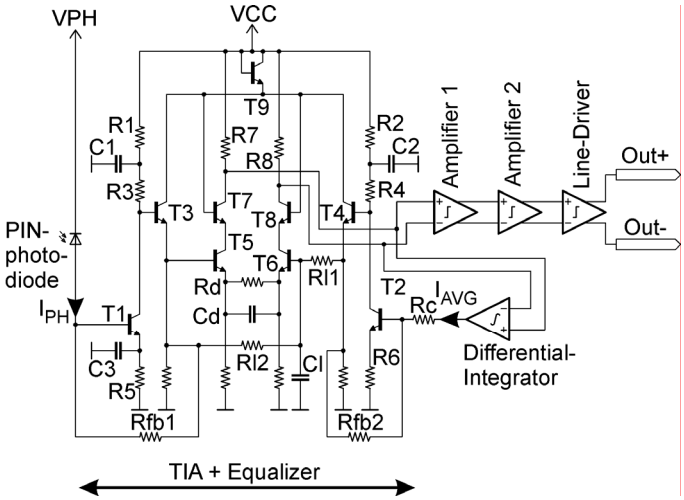

Figure 13.5.2: Simplified schematic of the receiver.

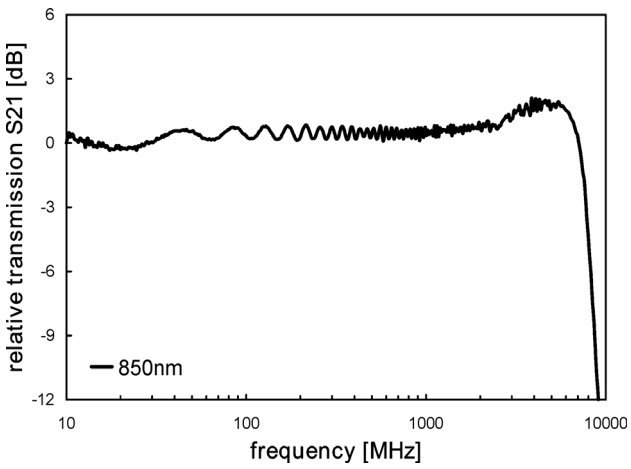

Figure 13.5.3: Frequency response of the receiver.

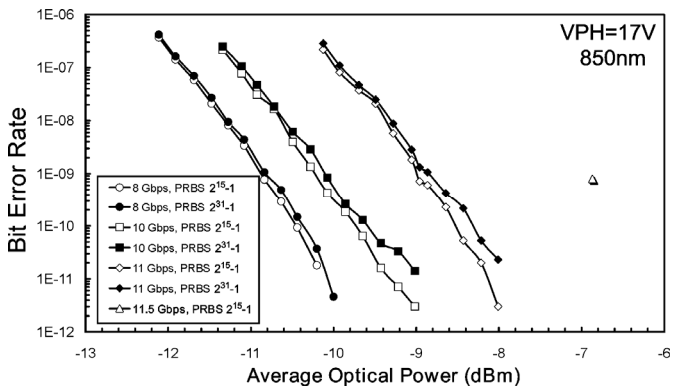

Figure 13.5.4: Bit error rate versus average optical power.

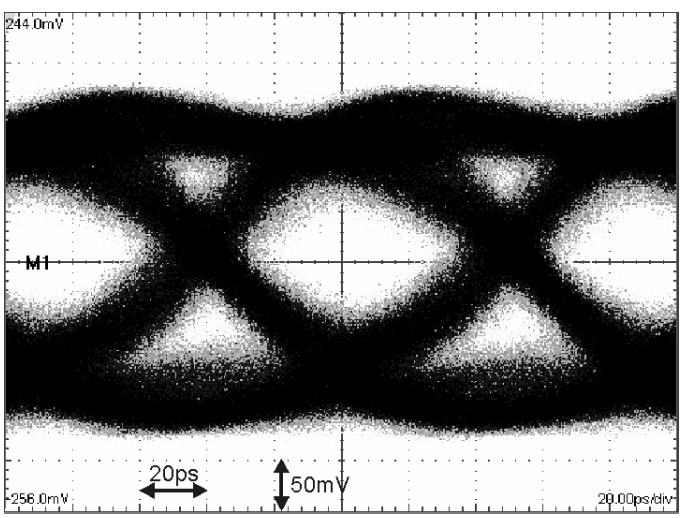

Figure 13.5.5: Eye diagram at 11Gb/s for 850nm and $P_{opt,avg}$=-8.9dBm, PRBS=2^{31}-1.

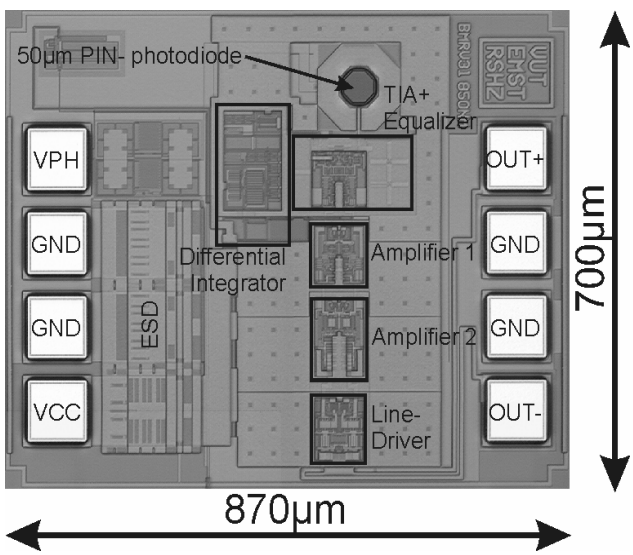

Figure 13.5.6: Chip micrograph of the complete receiver.